Freescale Semiconductor
Application Note

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MPC5121e SDHC Controller

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1 Introduction

The purpose of this application note is to describe the Secure Digital Host Controller implemented on Freescale's MPC5121e microcontroller. It describes how to configure and use the host controller with standard Secure Digital (SD™) cards, and how, through minor modifications in the existing software, driver support for High Capacity cards (SDHC™) can be added.

Portions of this application note were adapted from material found at the SD Association website, www.sdcard.org.

1.1 Objective

The objective of this application note is to describe the necessary steps needed to add support for SDHC cards.

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1.2 Definition of SDHC

The Secure Digital High Capacity card is the new Secure Digital memory card based on the version 2.00 specification (v. 2.0), released by the Secure Digital Association (SDA). This new specification introduces the ability to support SD cards capable of reaching higher capacities than before. The earlier SD standard, version 1.x, supported a memory size of up to 4 GB. The revised SDHC v.2.0 standard extends the supported capacity up to 32 GB. The new SDHC v.2.0 standard operates differently than standard SD v.1.x cards — this new format is not backwards-compatible with legacy SD-format host devices.

Products designed exclusively to support previous SD specifications v.1.x are not able to utilize SDHC format cards. (Note that the SD controller within the MPC5121e is designed according to SD specification v.1.x).

The SDHC specification v.2.0 calls for the card to be classified according to the minimal sustained Data Transfer Speed (DTS) as follows:

- Class 2: minimum sustained DTS of 2 MB/sec
- Class 4: minimum sustained DTS of 4 MB/sec
- Class 6: minimum sustained DTS of 6 MB/sec

SDHC cards are classified to guarantee a specific sustained DTS. This potentially saves consumers money, as flash cards are priced not only according to capacity, but also according to transfer speed. Devices that can utilize the 4 MB/s or 6 MB/s data transfer rates will offer significantly better performance when used with Class 4 or Class 6 SDHC cards.

The SDHC standard was developed by the Secure Digital Association (SDA) to address the requirement to support the growth in storage capacity of memory cards. The Secure Digital name was chosen because of the ability to protect copyright content through Digital Rights Management (DRM). As a result of this capability, it is a favored flash memory format in the audiovisual industry.

2 Description of Host

2.1 SD Host Controller in MPC5121e

The Secure Digital host controller module in the MPC5121e is capable of controlling MultiMedia Cards (MMC), Secure Digital cards (SD), and SD I/O cards.

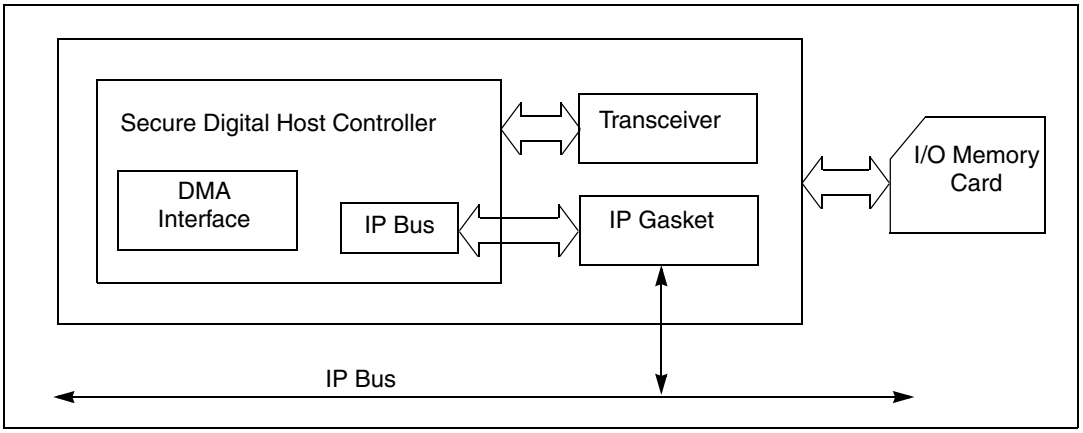

Figure 1. MPC5121e System Interconnection with the Secure Digital Host Controller

2.2 SD Host Controller Register List

The SD host controller available in the MPC5121e uses these registers for self-configuration and for communication with the connected card.

Table 1. SD Host Controller Register List

Address	Register
Base Address	SDHC Clock Control register (STR_STP_CLK)
Base Address + 04	SDHC Status register (STATUS)
Base Address + 08	SDHC Card Clock Rate register (CLK_RATE)
Base Address + 0C	SDHC Command Data Control register (CMD_DAT_CONT)
Base Address + 10	SDHC Response Time-Out register (RES_TO)
Base Address + 14	SDHC Read Time-Out register (READ_TO)
Base Address + 18	SDHC Block Length register (BLK_LEN)
Base Address + 1C	SDHC Number of Block register (NOB)
Base Address + 20	SDHC Revision Number register (REV_NO)
Base Address + 24	SDHC Interrupt Control register (INT_CNTR)
Base Address + 28	SDHC Command Number register (CMD)
Base Address + 2C	SDHC Command Argument register (ARG)
Base Address + 34	SDHC Command Response FIFO Access register (RES_FIFO)
Base Address + 38	SDHC Data Buffer Access register (DBA)

2.3 Signal Description and Connection Scheme

The Secure Digital Host Controller has six external pins. These are shown in Table 2.

Table 2. Signal Description

Signal	Description
MMC_SD_CLK	This signal is the MMC/SD/SDIO card clock signal. The direction is from host to card. The frequency is referenced to the system clock.
CMD	This is a bidirectional signal. It is for card initialization and data transfer commands.
DAT3	This is a bidirectional signal for data transmission in 4-bit mode. This signal is not used in 1-bit mode. This signal is also used for card detect in both 4-bit and 1-bit modes.
DAT2	This is a bidirectional signal for data transmission or read wait in 4-bit mode and is for read/wait when SDHC works in 1-bit mode.
DAT1	This is a bidirectional signal for data transmission or interrupt signal in 4-bit mode and is for interrupt signal when SDHC works in 1-bit mode.
DAT0	This is a bidirectional signal for data transmission in both 1-bit mode and 4-bit mode.

Figure 2 shows how the card is connected to host in 1-bit or 4-bit mode. The connection is the same for standard SD cards (v.1.x) and SDHC cards (v.2.0) as well.

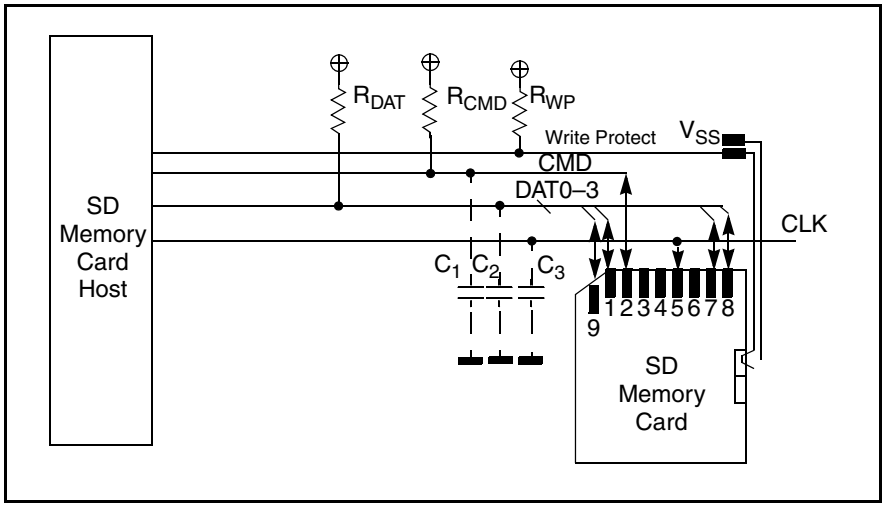

Figure 2. Connecting the SD/SDHC Card to the Host

2.4 Initialization

To assure proper host and card functionality, each module must be initialized before usage. When initializing the Secure Digital host controller, the user must obey these instructions.

2.4.1 IPS_BUS

When setting up a system with the MPC5121e, proper clocking must be assured. One of the important clock sources is the IPS_BUS clock. This clock can be as high as 83 MHz, but Freescale's recommendation is to use 66 MHz. It's used as a peripheral clock source. For example, it is used for the CAN, I^2C, timers, PCS's, SDH controller, etc.

2.4.2 MMC_SD_CLK

This clock is derived from the IPS_BUS clock. The default startup clock specified in the SD standard is 100 kHz. Depending on the card type, this clock can be set as high as 25 MHz according to the v.1.x specification, and can be set up to 50 MHz according to the v.2.0 specification. The actual highest clock rate has to be identified from the card configuration data. This data is stored in the card. The user must take care not to overclock the card. To set this clock, proper prescaler and divide values must be stored in the SDHC_CARD_CLOCK_RATE register. These values depend on the desired card clock and the host clock speed.

2.4.3 Timeout

As a part of the host setup, the user must set the appropriate timeouts for card operation. These timeouts are used to report problems while accessing the card. The highest and recommended values are:

- Response timeout SDHC_ RES_TO = 0xFF
- Read timeout SDHC_READ_TO = 0xFFFF

These values determine the interval which detects response and read timeout. The clock starts counting when the last bit of the command is sent.

2.4.4 Interrupts

If the user wishes to use interrupts instead of polling mode, the user must enable external interrupts to be passed to the core. The user must also enable interrupt from the SD host controller in the internal programmable interrupt controller (IPIC). Specific interrupt sources must be enabled in the Interrupt Control register (SDHC_INT_CNTR) in the SD host controller. These interrupts are used to acknowledge the completion of the send command, for example, “command done,” “read done,” “write done.” Interrupts are enabled by writing “1” to the proper position in the interrupt control register in the SD host controller and IPIC as well.

For further information on how to set the bus clock, SD host controller clocks, timeouts, enable interrupts, and handler interrupts refer to Freescale document MPC5121ERM, *MPC5121e Microcontroller Reference Manual*:

- Chapter 2, “System Configuration and Memory Map”
- Chapter 5, “Clocks and Low-Power Modes,” Section 5.3: “Clock Control Module”
- Chapter 20, “Integrated Programmable Interrupt Controller”
- Chapter 34, “Secure Digital Host Controller”

3 Description of Card

Before any communication with the card is done, it is absolutely necessary that the Secure Digital host controller be initialized. The SD host controller in the MPC5121e conforms to the SD specification v.1.x but can be forced to act and work as an SDHC capable controller. This is done during the card identification and initialization process, as shown in Figure 3 and Figure 4.

The main difference in the initialization compared to the old v.1.x standard is the use of CMD8. This command is not supported in the v.1.x specification and was introduced in the v.2.0 specification. It is used to identify SD/SDHC cards that conform to the Secure Digital v.2.0 specification. Cards that conform to the v.1.x specification will generate a timeout condition, or will reply with an error. Along with this command a new type of response was implemented, response R7. Although the SD host controller in the MPC5121e does not support response R7, a different but similar response can be used, R3.

Aside from the different initialization, the new protocol did include minor changes. One change is that the SDHC card uses physical sector addressing (similar to ATA disk drives), but the SD cards use memory addressing (similar to RAM).

Also, the SECTOR_SIZE was set to 512 bytes, in contrast to the variable size as described in v.1.x. To assure compatibility and ease of use, it is recommended to use the same sector size with each card type.

For more information see the complete specification from the Secure Digital Association (SDA) at www.sdcard.org.

3.1 Initialization

The steps in the figures are numbered and correspond to the steps given after the figures.

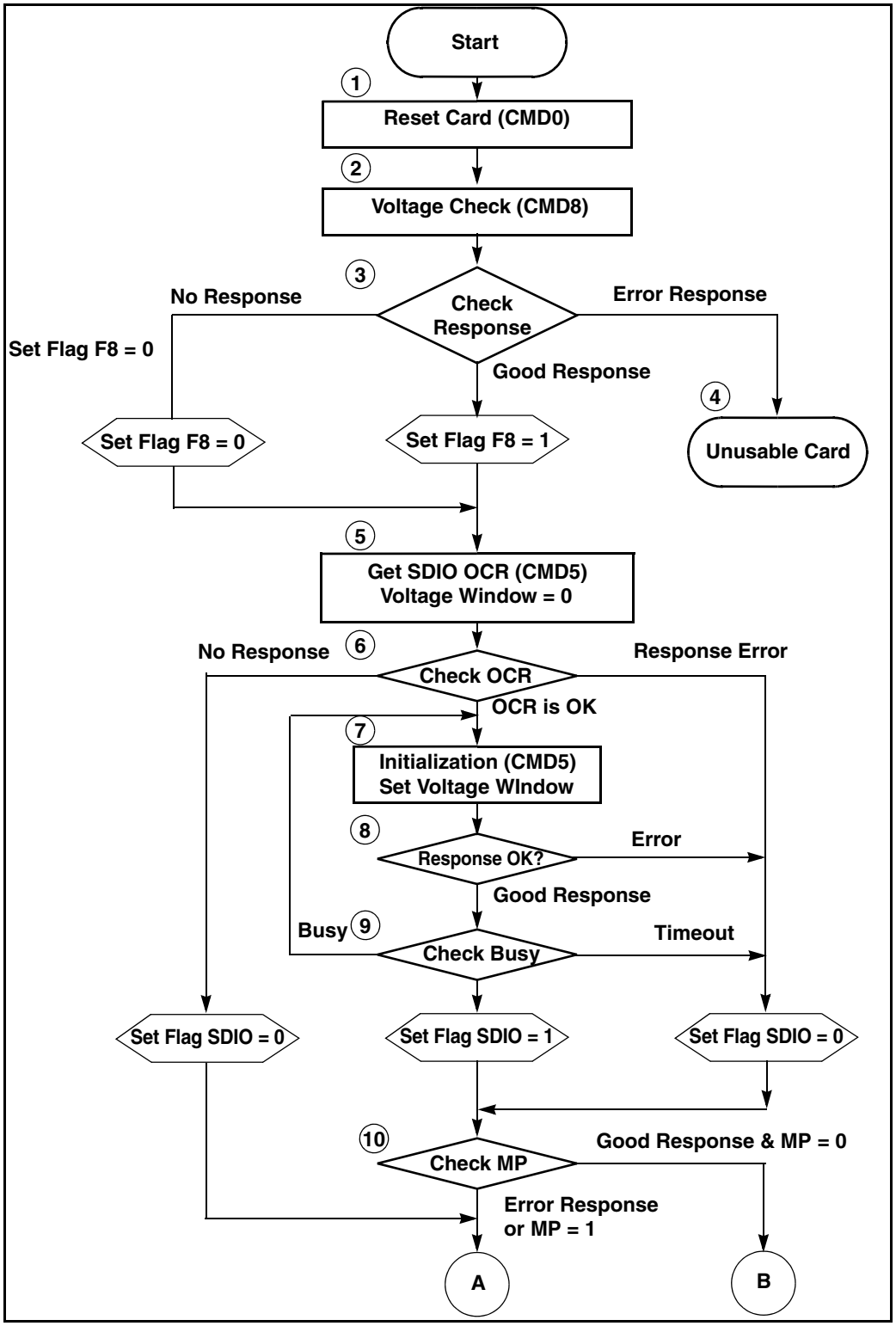

Figure 3. New Initialization Described in V.2.0 Specification — Part 1 of 2

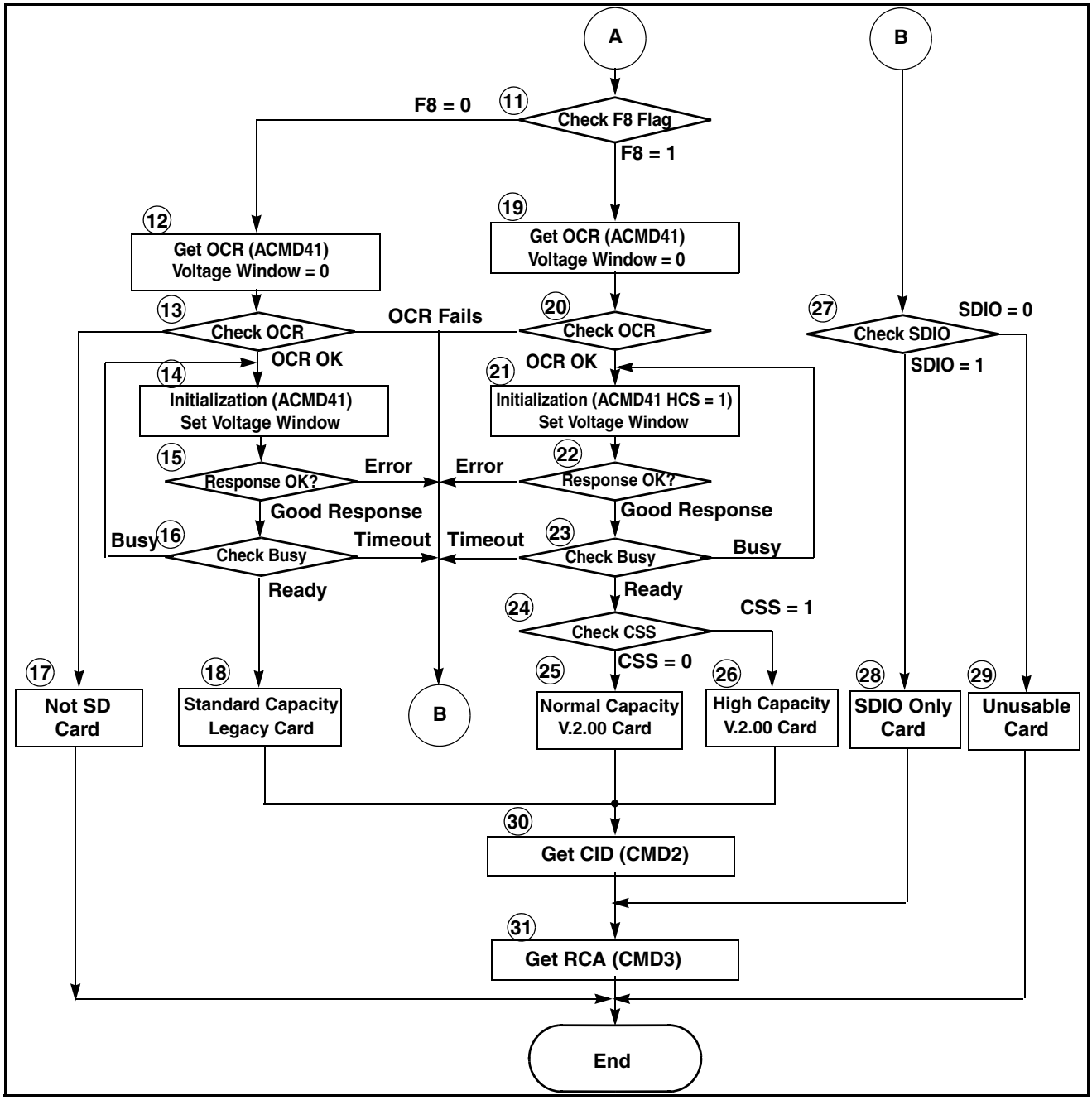

Figure 4. New Initialization Described in V.2.0 Specification — Part 2 of 2

1. SD bus mode is selected by CMD0 (card reset).
2. New CMD8 shall be issued after CMD0 to support High Capacity SD memory card.
3. Voltage check command enables the hosts to support future low-voltage specification. However, at this time only one voltage is defined. Legacy cards and non-SD cards do not respond to CMD8. In this case, set F8 to 0 (F8 is CMD8 valid flag used in step 11) and go to step 5. Only version 2.00 or higher cards can respond to CMD8. The host needs to check whether CRC of the response is valid, and whether host-supplied voltage range (VHS) and check pattern in the argument are equal

to card-accepted voltage range (VCA) and check pattern in the response. Passing all these checks results in CMD8 response OK. In this case, set F8 to 1 and go to step 5. If one of the checks fails, go to step 4.

4. Initialization is stopped if CMD8 fails. The host driver should retry steps 1 to 3 one more time. (This is not described in Figure 3).
5. SDIO Operation Condition register (OCR) is available by issuing CMD5 and setting the voltage window (bits 23 to 0) in the argument to 0. SDIO initialization is not started. The OCR contains the information about the supported voltage and the card's condition, either active or inactive.
6. No response means the card does not have the SDIO function. Set SDIO flag to 0 and go to step 11. If the card responds to CMD5 and the response is OK, go to step 7. If the response indicates error, set SDIO flag to 0 and go to step 10. The SDIO flag indicates whether SDIO functions are initialized or not.
7. The SDIO portion starts initialization by CMD5 and sets the supply voltage to the voltage window. If the supplied voltage does not match the voltage window of the card, the card goes into inactive state and does not return the response.
8. If no response or error response is received, set SDIO flag to 0 and go to step 10. If a valid response is received, go to step 9.
9. Check busy status in the response. If busy status is negative, set the SDIO flag to 1 and go to step 10. Repeat from step 7 while busy is indicated. Detecting a timeout of 1 second exits the loop. In this case, set SDIO flag to 0 and go to step 10.
10. Good response in this step means that all responses received at (6) and (8) are valid. When response is good, MP (memory present) flag in the response can be checked. If the response is valid and MP = 0, go to step 28. Otherwise, go to step 11.
11. Check F8 flag that was set in step 3. If CMD8 is executed correctly (F8 = 1), go to step 19. Otherwise, go to step 12.
12. OCR is available by issuing ACMD41 with the voltage window (bit 23 to 0) in the argument set to 0. Memory initialization is not started. A response of CMD55 (ACMD41) may indicate illegal command error, because some SD cards do not recognize CMD8. The host driver should ignore this error or issue CMD0 before ACMD41 to clear this error status.
13. If a response of CMD55 is not received, the card is not an SD card and processing goes to step 17. If the card responds to CMD55, it may also respond to CMD41. If the responses of ACMD41 are OK, go to step 14. Otherwise, go to step 27. A locked card can be detected by the card status in the response of CMD55.
14. The memory portion starts initialization by issuing ACMD41 and setting the supply voltage to the voltage window. If the supplied voltage does not match the voltage window of the card, the card goes into inactive state and does not return the response.
15. If no response or error response is received, go to step 27. If a good response is received, go to step 16.
16. Check busy status in the response. If busy is released, go to step 18. Repeat from step 14 while a status of busy is indicated. The interval of ACMD41 must be less than 50 ms. Detecting a timeout of 1 second exits the loop and goes to step 27.
17. The host recognizes that the card is not an SD memory card and quits SD card initialization.

18. The host recognizes that the card is a v.1.x Standard Capacity SD memory card. Go to step 30.
19. OCR is available by issuing ACMD41 and setting the voltage window (bits 23 to 0) in the argument to 0. Memory initialization is not started. A setting of High Capacity Support (HCS) does not affect this operation.
20. If the card responds to CMD55, it may also respond to CMD41. If the responses of ACMD41 are OK, go to step 21. Otherwise, go to step 27. A locked card can be detected by the card status with a response of CMD55.
21. The memory portion starts initialization by issuing ACMD41 and setting the supply voltage to the voltage window. If the supplied voltage does not match the voltage window of the card, the card goes into an inactive state and does not return the response. HCS in the argument is set to 1, which indicates supporting High Capacity Memory Card. This is the part where we force the SD host controller to identify itself as SDHC capable, even when it is not. The default should be 0.
22. If no response or an error response is received, go to step 27. If a good response is received, go to step 23.
23. Check busy status in the response. If busy is released, go to step 24. Repeat from step 21 while a status of busy is indicated. The interval of ACMD41 must be less than 50 ms. Detecting a timeout of 1 second exits the loop and goes to step 27.
24. CCS in the response is valid after busy is released. If CCS = 0, it indicates the Standard Capacity SD memory card and processing goes to step 25. If CSS = 1, it indicates the High Capacity SD memory card and processing goes to step 26. This information is stored in the OCR.
25. The host recognizes that the card is a Standard Capacity SD memory card. Optimal functions defined in v.2.0 or higher are available. Go to step 30.
26. The host recognizes that the card is a High Capacity SD memory card. Go to step 30.
27. Check SDIO flag. If SDIO=1, go to step 28. Otherwise, go to step 29.
28. The host recognizes that the card is an SDIO-only card. Go to step 31.
29. The host recognizes that the card is unusable.
30. In the case of a memory card, CMD2 is issued to get card identification (CID) and processing goes to step 31. The CID contains information about the vendor, serial number, manufacturing date, etc.
31. CMD3 is issued to get Relative Card Address (RCA). If the RCA number is 0, the host should issue CMD3 again.

3.2 Read/Write Procedures

Until the content of the Card Specific Data (CSD) register is known by the host, the card clock rate must remain at 100 kHz, because some cards may have operating frequency restrictions. The host issues SEND_CSD (CMD9) to obtain the CSD register, for example block length, card storage capacity, and maximum clock rate. Figure 5 shows a block diagram of the Data Transfer mode.

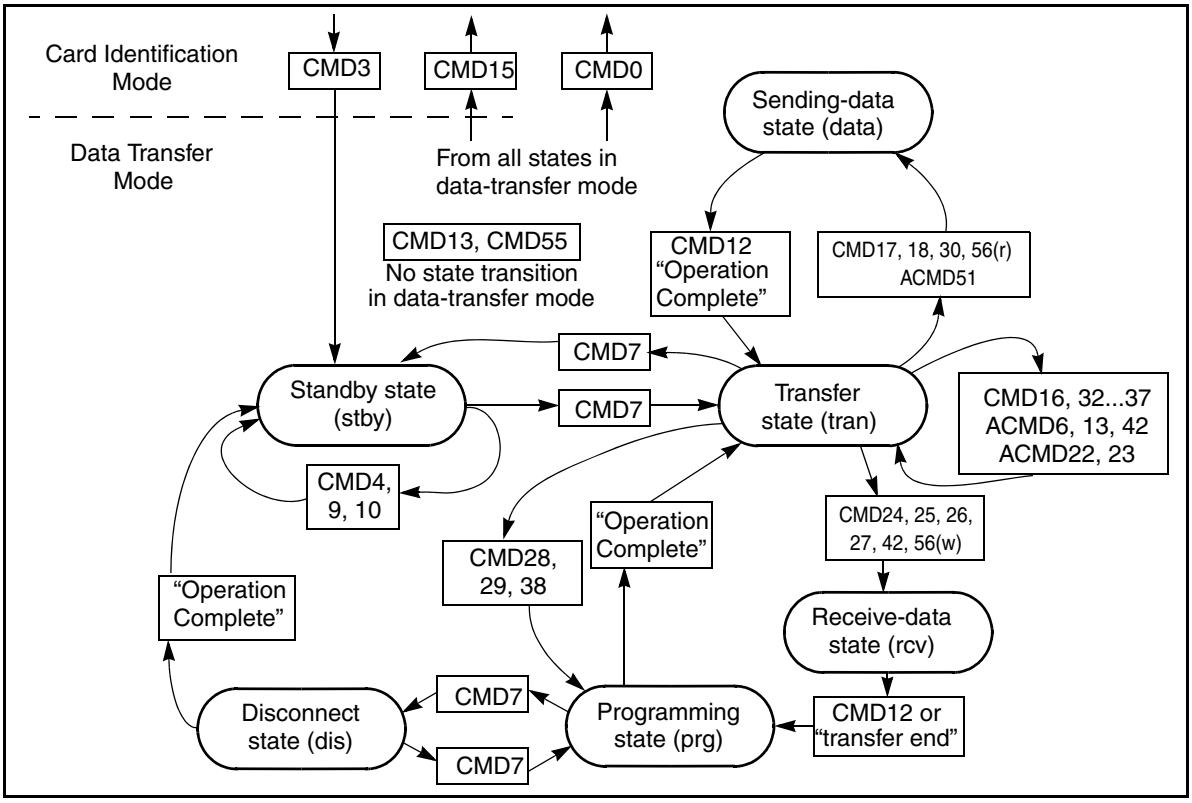

Figure 5. Description of Card States

CMD7 is used to select one SD card and place it in the transfer state. Only one SD card can be in the transfer state at a given time. If a previously selected SD card is in the transfer state, its connection with the host is released and it will move back to the standby state. When CMD7 is issued with the reserved relative card address "0x0000," all cards transfer back to standby state. (Note that it is the responsibility of the host to reserve RCA = 0 for card deselection). This may be used before identifying new cards without resetting other already registered cards. Cards that already have an RCA do not respond to identification commands (ACMD41, CMD2, CMD3) in this state.

NOTE

The card deselection is done if a certain card gets CMD7 with unmatched RCA. That happens automatically if selection is done to another card and the CMD lines are common. So, in the SD card system, it will be the responsibility of the host either:

- To work with the common CMD line (after initialization is done); in this case the card deselection will be done automatically (as in MultiMediaCard system).
- Or if the CMD lines are separate, to be aware of the necessity to deselect cards.

All data communication in the data transfer mode is point-to-point between the host and the selected SD card (using addressed commands). All addressed commands are acknowledged with a response on the CMD line. The relationship between the various data transfer modes is summarized in Figure 5, and in the following paragraphs:

- All data read commands may be aborted any time by the stop command (CMD12). The data transfer will terminate and the card will return to the transfer state. The read commands are: block read (CMD17), multiple block read (CMD18), send write protect (CMD30), send SCR (ACMD51) and general command in read mode (CMD56).
- All data write commands can be aborted any time by the stop command (CMD12). The write commands must be stopped prior to deselecting the card by CMD7. The write commands are: block write (CMD24 and CMD25), write CID (CMD26), write CSD (CMD27), lock/unlock command (CMD42), and general command in write mode (CMD56).
- As soon as the data transfer is completed, the card will exit the data write state and move either to the programming state (transfer is successful) or transfer state (transfer failed).
- If a block write operation is stopped and the block length and CRC of the last block are valid, the data will be programmed.
- The card may provide buffering for block write. This means that the next block can be sent to the card while the previous block is being programmed. If all write buffers are full, and as long as the card is in programming state, the DAT0 line will be kept low (BUSY).
- There is no buffering option for write CSD, write CID, write protection, or erase. This means that while the card is busy servicing any one of these commands, no other data transfer commands will be accepted. The DAT0 line will be kept low as long as the card is busy and in the programming state. Note that if the CMD and DAT0 lines of the cards are kept separated and the host keeps the busy DAT0 line disconnected from the other DAT0 lines (of the other cards), the host may access the other cards while the card is busy. Parameter set commands are not allowed while the card is programming. Parameter set commands are: set block length (CMD16), erase block start (CMD32), and erase block end (CMD33).
- Read commands are not allowed while the card is programming.
- Moving another card from standby to transfer state (using CMD7) will not terminate erase and programming operations. The card will switch to the disconnect state and will release the DAT line.
- A card can be reselected while in the disconnect state using CMD7. In this case the card will move to the programming state and reactivate the busy indication.
- Resetting a card (using CMD0 or CMD15) will terminate any pending or active programming operation. This may destroy the data contents on the card. It is the host’s responsibility to prevent this.

4 SDA Host and Card Specifications

4.1 Environmental

Table 3. Environmental Specification

Temperature	Operating Non-operating	–25 °C to 85 °C –40 °C to 85 °C
Humidity	Operating Non-operating	25% to 95%, non-condensing 25% to 95%, non-condensing
ESD protection	Contact Pads	±4k V, human body model according to ANSI EOS/ESD-S5.1-1998
	Non-Contact Pad Area	±8k V (coupling plane discharge) ±15k V (air discharge) Human body model per IEC61000-4-2

4.2 Reliability and Durability

Table 4. Reliability and Durability Specification

Durability	10,000 mating cycles
Bending	10 N
Torque	0.15 N.m or ±2.5 deg.
Drop Test	1.5 m free fall
UV Light Exposure	UV: 254 nm, 15Ws/cm2 according to ISO 7816-1
Visual Inspection/Shape and Form	No warpage; no mold skin; complete form; no cavities; surface smoothness –0.1 mm/cm^2 within contour; no cracks; no pollution (oil, dust, etc.)
Minimum Moving Force of WP Switch	40 gf (ensures that the WP switch will not slide while it is inserted in the connector)
WP Switch Cycles	Minimum 1,000 Cycles @ slide force 0.4 N to 5 N

4.3 Power Supply

Table 5. Power Supply Specification

Peak Voltage on All Lines	–0.3	Supply voltage +0.3	V	
Input Leakage Current	–10	10	mA	All inputs
Output Leakage Current	–10	10	mA	All outputs
Supply Voltage	2.0	3.6	V	CMD0, 15, 55, ACMD41 commands
Supply Voltage	2.7	3.6	V	Except CMD0, 15, 55, ACMD41 commands
Power-Up Time		250	ms	From 0 V to V_{DD} min.

5 References

1. MPC5121ERM, *MPC5121e Microcontroller Reference Manual*

2. Secure Digital Association website www.sdcard.org

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